REMARKS

This paper is responsive to a non-final Office action dated July 23, 2004. Claims 1-12 and 47-69 were examined. The Examiner rejected all claims. Claims 1, 47, 55, 59, and 69 have been amended, but not to overcome any art of record.

Rejections under 35 U.S.C. §112

The Office has rejected claims 1 – 12 and 47 – 69 under 35 U.S.C. §112 as being indefinite for failing to particularly point and distinctly claim the subject matter which Applicant regards as the invention. The Office has specifically referred to independent claims 1, 47, 55, 59, 63, and 69. Claims 1, 47, 55, 59, and 69 have been amended.

The Office states that "it is not clear how the faulting memory location can be reserved." The specification at paragraph 1024, section 8 describes an exemplary scenario of a fault being signaled if a value V_1 read from a reserved memory location A_1 is equal to a comparison value C_1 and if the memory location A_2 was previously determined to be invalid.

Claim 1 has been amended to recite "a later one of the respective locations depends on a value read from an earlier reserved one of the respective locations." Claim 43 has been similarly amended. Claim 55 has been amended to recite "selectively signaling a fault corresponding to the second one of the memory locations depending on a result of the first memory location access." Claim 59 has been amended to recite "addresses the first and second memory locations but for which signaling of a fault corresponding to the second memory location depends on a value read from the first reserved memory location." Claim 69 has been amended to recite "means for signaling, if at all, a fault corresponding to the second location based on a value read from the reserved first location."

Claim 63 does not claim reservation of a faulting memory location as asserted by the Office. Claim 63 recites that "at least one instance of an instruction ***directing the processor to separately reserve first and second memory locations*** prior to accessing contents of either of the first and second memory locations, and to access first and second memory locations but for which signaling of a fault corresponding to the second memory location depends on a value read from the first memory location." Claim 63 does not require that both memory locations be

reserved. Although the instruction instance directs the processor to separately reserve the memory locations, the processor may fail to reserve the second memory location. Hence, the first memory location may be reserved while the second memory location is not reserved.

Conclusion

In summary, claims 1 – 12 and 47 – 69 are in the case. All claims are believed to be allowable over the art of record, and a Notice of Allowance to that effect is respectfully solicited. Nonetheless, if any issues remain that could be more efficiently handled by telephone, the Examiner is requested to call the undersigned at the number listed below.

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Steven R. Gilliam — Oct-20-2004 (Date)

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Respectfully submitted,

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